ABSTRACT:

System (50), e.g. a System on a chip (SoC), comprising a system bus (56), a high-speed functional block (51) operably linked to the system bus (56), and a high-speed clock line (54) for applying a high-speed clock to the high-speed functional block (51). The system (50) further comprises a peripheral bus (59), a low-speed functional block (52) operably linked to this peripheral bus (59), a circuitry (53) for generating a wait signal (PWAIT), a low-speed clock line (57) for applying a low-speed clock (PCLK) to the low-speed functional block (52), a select line (58) for feeding a select signal (PSEL) from the peripheral bus (59) to the low-speed functional block (52), an enable line (55) for applying a clock enable signal (PCLKEN) to the circuitry (53), and a wait line (61) for feeding the wait signal (PWAIT) to the high-speed functional block (51). The circuitry (53) generates the wait signal (PWAIT) from the select line signal (PSEL) and the clock enable signal (PCLKEN).

(Fig. 2)